REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Office Action, Claims 1-5 and 7-16 stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by U.S. Patent No. 6,458,695 to Lin, et al. (Lin, et al.").

In response to the anticipation rejection under 35 U.S.C. §102(e), applicants refer to the attached 131 Declaration (including Exhibits A and B) that accompanies the submission of this Response. In the attached 131 Declaration, the applicants have declared that they have conceived and reduced to practice the invention, which is disclosed and claimed in the present application, prior to the effective filing date of Lin, et al. (i.e., prior to October 18, 2001). Specifically, the applicants have declared that they have conceived and reduced to practice a semiconductor structure such as, a metal oxide semiconductor (MOS) or field effect transistor (FET), that includes a semiconductor substrate having source and drain regions, a gate dielectric having a thickness of less than 100 Å on the semiconductor substrate; and a gate formed of a metal comprising Re on top of the gate dielectric, as is recited in Claims 1 and 10 of the present application. To evidence the conception and reduction to practice of the claimed structure, the 131 Declaration includes Exhibits A and B. Exhibit A is a true photocopy of IBM Invention Disclosure YOR820010675, which was created prior to October 18, 2001. This exhibit includes a Main Ideal section for the Invention Disclosure which describes the fabrication of a semiconductor structure such as, a MOS or FET, that includes Re as the gate electrode. Exhibit B is the inventors' write-up of the Disclosure that was also created prior to the effective filing date of Lin, et al. This write-up provides greater detail of the invention presently claimed. Particular attention is made to the experimental data in

Exhibit B that establishes clear evidence of actual fabrication of the semiconductor structures presently claimed.

In view of the above together with the submission of the accompanying 131 Declaration, applicants respectfully submit that the rejection of Claims 1-5 and 6-17 under 35 U.S.C. §102(e) citing Lin, et al. has been obviated.

Thus, in view of the foregoing remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

Leslie S. Szivos
Registration No. 39,394

Scully, Scott, Murphy & Presser
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343

LSS:gc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Ricky Amos, et al.

Examiner: Matthew C. Landau

Serial No: 09/995,031

Art Unit: 2815

Filed: November 29, 2001

Docket: YOR92001063US1 (19031)

For: HIGH TEMPERATURE PROCESSING COMPATIBLE METAL GATE ELECTRODE FOR pFETs AND METHOD FOR FABRICATION

Dated: July 26, 2005

Confirmation No: 9669

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION PURSUANT TO 37 C.F.R. §1.131

Sir:

We, Ricky Amos, Douglas A. Buchanan, Cyril Cabral, Jr., Alessandro C. Callegari, Supratik Guha, Hyungjun Kim, Fenton R. McFeely, Vijay Narayanan, Kenneth Rodbell, and John J. Yurkas, hereby declare that:

1. We are co-inventors of the subject matter described and claimed in the above-identified patent application.

2. Prior to October 18, 2001, which is the effective filing date of U.S. Patent No. 6,458,695 to Lin, et al. ("Lin, et al."), we have conceived and reduced to practice a semiconductor structure such as, a metal oxide semiconductor (MOS) or a field effect transistor (FET), that includes a semiconductor substrate having source and drain regions, a gate dielectric having a thickness of less than 100 Å on the semiconductor substrate; and a

gate formed of a metal comprising Re on top of the gate dielectric, as is recited in Claims 1 and 10 of the present application.

3. As evidence of the conception and reduction to practice of the claimed semiconductor structure referred to in paragraph 2 prior to the effective filing date of Lin, et al., annexed hereto are Exhibits A and B. Exhibit A is a true photocopy of IBM Invention Disclosure YOR820010675, which was created prior to October 18, 2001. Exhibit A includes a Main Ideal section for the Invention Disclosure which describes the fabrication of a semiconductor structure such as a MOS or FET that includes Re as the gate electrode. Exhibit B is the inventors' write-up of the Disclosure that was also created prior to the effective filing date of Lin, et al. This write-up provides greater detail of the invention presently claimed including experimental data that establishes clear evidence of actual fabrication of the claimed semiconductor structure . All names and dates have been redacted in the preparation of this Declaration.

4. We do hereby declare that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

July 26, 2005
Dated

Ricky Amos

July 25, 2005
Dated

Douglas A. Buchanan

July 25, 2005
Dated

Cyril Cabral, Jr.

C:\Documents and Settings\D Buchanan\Local Settings\Temporary Internet Files\OLKD\U903J declaration.doc

7/26/05
Dated

Alessandro C. Callegari

7/26/05
Dated

Supratik Guha

7/23/05
Dated

Hyungjun Kim

7/23/05
Dated

Fenton R. McFeely

07/26/05
Dated

Vijay Narayanan

7/26/2005
Dated

Kenneth P. Rodbell

7/26/2005
Dated

John J. Yurkas

Applicant(s): Ricky Amos, et al.

Examiner: Matthew C. Landau

Serial No: 09/995,031

Art Unit: 2815

Filed: November 29, 2001

Docket: YOR92001063US1 (19031)

For: HIGH TEMPERATURE PROCESSING
COMPATIBLE METAL GATE ELECTRODE
FOR pFETs AND METHOD FOR FABRICATION

Confirmation No: 9669

Exhibit A

Disclosure YOR8-2001-0675

Prepared for and/or by an IBM Attorney - IBM Confidential

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

*Title of disclosure (in English)

High Temperature processing compatible metal gate electrode for p-fet's and method for its fabrication

Summary

Status	Final Decision (File)
Final deadline	
Final deadline reason	
Docket family	YOR9-2001-0633
* Processing location	Yorktown
* Functional area	(700) 700 Isaac-Systems, Technology & Science
Attorney/Patent professional	
IDT team	
Submitted date	
* Owning division	RES
Incentive program	
Lab	
* Technology code	
Patent value tool (PVT) score	47

Inventors without a Blue Pages entry

IDT Selection

Main Idea

To view the Main Idea of this disclosure, open the "Main Idea" document from the view

*Critical Questions (Questions 1-9 must be answered in English)

*Question 1
On what date was the invention workable? Please format the date as MM/DD/YYYY
(Workable means i.e. when you know that your design will solve the problem)

*Question 2
Is there any planned or actual publication or disclosure of your invention to anyone outside IBM? ● Yes ○ No

If yes, Enter the name of each publication or patent and the date published below.

Date Published or Issued: publication planned at some unspecified future time

Are you aware of any publications, products or patents that relate to this invention? ○ Yes ● No

If yes, Enter the name of each publication or patent and the date published below.
Publication/Patent:
Date Published or Issued:

*Question 3
Has the subject matter of the invention or a product incorporating the invention been sold, used internally in manufacturing, announced for sale, or included in a proposal? ○ Yes ● No

Is a sale, use in manufacturing, product announcement, or proposal planned? ○ Yes ● No

If Yes, identify the product if known and indicate the date or planned date of sale, announcements, or proposal and to whom the sale, announcement or proposal has been or will be made.
Product:
Version/Release:
Code Name:
Date:
To Whom:
If more than one, use cut and paste and append as necessary in the field provided.

*Question 4
Was the subject matter of your invention or a product incorporating your invention used in public, e.g., outside IBM or in the presence of non-IBMers? ○ Yes ● No

If yes, give a date. Please format the date as MM/DD/YYYY

*Question 5
Have you ever discussed your invention with others not employed at IBM? ○ Yes ● No

If yes, identify individuals and date discussed. Fill in the text area with the following information, the names of the individuals, the employer, date discussed, under CDA, and CDA #.

*Question 6
Was the invention, in any way, started or developed under a government contract or project? ○ Yes ● No ○ Not sure

If Yes, enter the contract number

*Question 7
Was the invention made in the course of any alliance, joint development or other

contract activities? ○ Yes ● No ○ Not Sure

If Yes, enter the following:

	Name of Alliance, Contractor or Joint Developer
	Contract ID number
	Relationship contact name
	Relationship contact E-mail
	Relationship contact phone

*Question 8
Have you, or any of the other inventors, submitted this same invention disclosure or similar invention disclosure previously? ○ Yes ● No

If Yes, please provide disclosure number below:

*Question 9
Are you, or any of the other inventors, aware of any related inventions disclosures submitted by anyone in IBM previously? ○ Yes ● No

If Yes, please provide the docket or disclosure number or any other identifying information below:

Question 10
What type of companies do you expect to compete with inventions of this type? *Check all that apply.*

- ☒ Manufacturers of enterprise servers
- ☒ Manufacturers of entry servers
- ☒ Manufacturers of workstations
- ☒ Manufacturers of PC's
- ☒ Non-computer manufacturers
- ☐ Developers of operating systems
- ☐ Developers of networking software
- ☐ Developers of application software
- ☐ Integrated solution providers
- ☐ Service providers
- ☐ Other (Please specify below)

Question 11
If the invention relates to a product or service that is outside the scope of your business unit, please recommend IBM business unit(s), IBM location(s) or individual(s) within IBM that you think would provide a good evaluation of your invention:
N/A

*Patent Value Tool (Optional - this may be used by the inventor and attorney to assist with the evaluation

(The Patent Value tool can be used by the inventor(s) to determine the potential licensing value of your invention.)
Market
*Question 1: What is the anticipated annual market size (in dollars) that will be captured by your invention?

$1B to $5B
Reason(s) for above Answer: could become standard method for future CMOS

Claims
*Question 1: How new is the technical field?
Emerging
Reason(s) for above Answer: metal gates are not currently in use with CMOS, but planning for thier incorporation is active.

*Question 2: How central is the invention to the product(s) which might be expected to contain the invention?
Essential
Reason(s) for above Answer: a suitable gate electrode for pFET's is esential for functioning CMOS technology

*Question 3: What is the scope of the claim?
Broad
Reason(s) for above Answer:

Portfolio Need
*Question 1: What are the portfolio needs in the area of your invention?
Listed in PPM Needs
Reason(s) for above Answer: pertains to advanced CMOS devices, PPM 100, A2

Exploitation & Enforcement
*Question 1: How easily can the use of the invention by a competitor be detected?
With work
Reason(s) for above Answer: straight forward sims or equivalent chemical analysis will reveal the presence of Re

*Question 2: How easily can the use of the invention be avoided by a competitor?
With much work
Reason(s) for above Answer: entirely new, low temperature processing schemes might have to be developed

Business Value
*Question 1: What percentage of the companies producing products in the field of this invention might use this invention?
Broadly cloned
Reason(s) for above Answer: it could become the standard form of CMOS, equivalent to the poly gates of today

*Question 2: What is the value of this patent to current or anticipated Alliance Activity between IBM and other companies?
Some value
Reason(s) for above Answer: not really known

*Question 3: What is the value of this patent to current or anticipated Technology Transfer Activity between IBM and other companies?
High value
Reason(s) for above Answer:

*Question 4: Does it result in prestige to IBM?
Industry wide
Reason(s) for above Answer: if it becomes the industry standard

Final Decision

This decision was entered by

Decision: File	Status: N/A
PPM area:	
Date of final decision :	

Additional filing information
Planned Filing date:
Filing comments:

Additional decision comments

Final Decison History

Post Disclosure Text & Drawings

To add additional information related to this disclosure once it has been submitted, click the action button below and a new document will be opened for you to enter the new information. To view existing post disclosure information, double-click on the item in the list below (if there has been additional information entered), and the document will open for you to view.

Date entered	Post disclosure comments and drawings (double-click an item below to view)

Main Idea for Disclosure YOR8-2001-0675

Prepared for and/or by an IBM Attorney - IBM Confidential

Title of disclosure (in English)
High Temperature processing compatible metal gate electrode for p-fet's and method for its fabrication

Main Idea

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.
The invention is the fabrication of a gate electrode comprising Re metal. The work fucnction of Re makes it compatible with current pFET requirements. As it is elemental in nature, it can withstand the high hydrogen pressures necessary to produce properly passivated interfaces without undergoing chemical changes. Its thermal stabiliy on SiO2 Al2O3 and a variety of other dielectrics makes it comptible with post processing temperatures up to 1000 C. Methods have been developed to fabricate fet's and to passivate the channel/dielectric interfaces of these fet's to better than 5e10 interface states/cm2

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?
The new pfet gate avoids the problem of poly depletion which reduces the effective capacitance of poly gate devices, and necessitates the use of a thinner dielectric than would otherwise be required. At the same time its thermal stability makes it fully compatible with satndard post processing techniques, e,g. acitvation anneals and the like.

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?
the problem is generally known, but there are no fully satisfactory solutions extant.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.
N/A

Applicant(s): Ricky Amos, et al.

Examiner: Matthew C. Landau

Serial No: 09/995,031

Art Unit: 2815

Filed: November 29, 2001

Docket: YOR92001063US1 (19031)

For: HIGH TEMPERATURE PROCESSING COMPATIBLE METAL GATE ELECTRODE FOR pFETs AND METHOD FOR FABRICATION

Confirmation No: 9669

Exhibit B

***Main Idea**

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

The invention is the fabrication of a CMOS gate electrode comprising a Re, Rh, Pt, Ir or Ru metal. The work functions of Re, Rh, Pt, Ir or Ru make them compatible with current pFET requirements. The

requirements of the pFET gate material along with experimental results are described below. The requirements are divided into four sections physical characterization, deposition techniques, electrical characterization and integration.

Physical characterization - Depending on the integration scheme thermal stability (preferably up to 1000 C) from agglomeration, from reaction with the dielectric (formation of an interlayer between the gate metal and dielectric) and reaction with the annealing ambient (forming gas (FG) or hydrogen (H)) is required of the metal gate material. A second requirement is low resistivity, 1-2 mOhm-cm for the gate contact and more preferably lower than 50 micro Ohm-cm for gate contact plus local interconnect use (like what is currently practiced with silicides). Rhenium has a resistivity lower than 50 micro Ohm-cm after a 1000 C FG anneal treatment on both SiO_2 and Al_2O_3 dielectrics.

The thermal stability of various gate materials in contact with both SiO_2 and Al_2O_3 dielectrics were investigated using three techniques employed at the Brookhaven National Laboratory, National Synchrotron Light Source. The techniques include time resolved x-ray diffraction analysis used to determine if the metal electrode undergoes an interaction with the dielectric layer or FG annealing ambient, optical scattering and resistance analysis as a function of temperature used to determine if the film undergoes agglomeration or thermal degradation. All three techniques were monitored simultaneously while the samples were heated from 100 to 1000 C in FG. It was determined that for the stack of 30 nm Re, Rh, Pt or Ir on 500 nm SiO_2 or 300 nm Al_2O_3 there was no thermal degradation or reactions during the anneal treatments. The two graphs below show the results from the 50 nm CVD Re / 500 nm SiO_2 and 30 nm PVD Re / 300 nm Al_2O_3 stacks annealed to 1000 C in FG.

Figure 1 below shows the results from annealing a 50 nm CVD Re film on 500 nm SiO_2 in FG at 3 C/s up to 1000 C. The contour plot (diffraction angle vs. temperature with color scale indicating x-ray intensity, dark blue lowest intensity and dark red highest intensity) follows the (002) orientation of Re as a function of temperature. Notice the peak linearly moves to lower angles on annealing due to lattice expansion and at about 750 C the intensity increases indicating grain growth in the film. There are no indications of additional peaks or a decrease in intensity of the (002) peak which would signify a reaction with the dielectric or annealing ambient. The top plot shows the optical scattering analysis at two different lateral length scales (0.5 and 5 micro meters, red and blue curves respectively). Changes would indicate surface roughness developing in the film leading to thermal degradation. In this case no changes are seen indicating the film is not agglomerating.

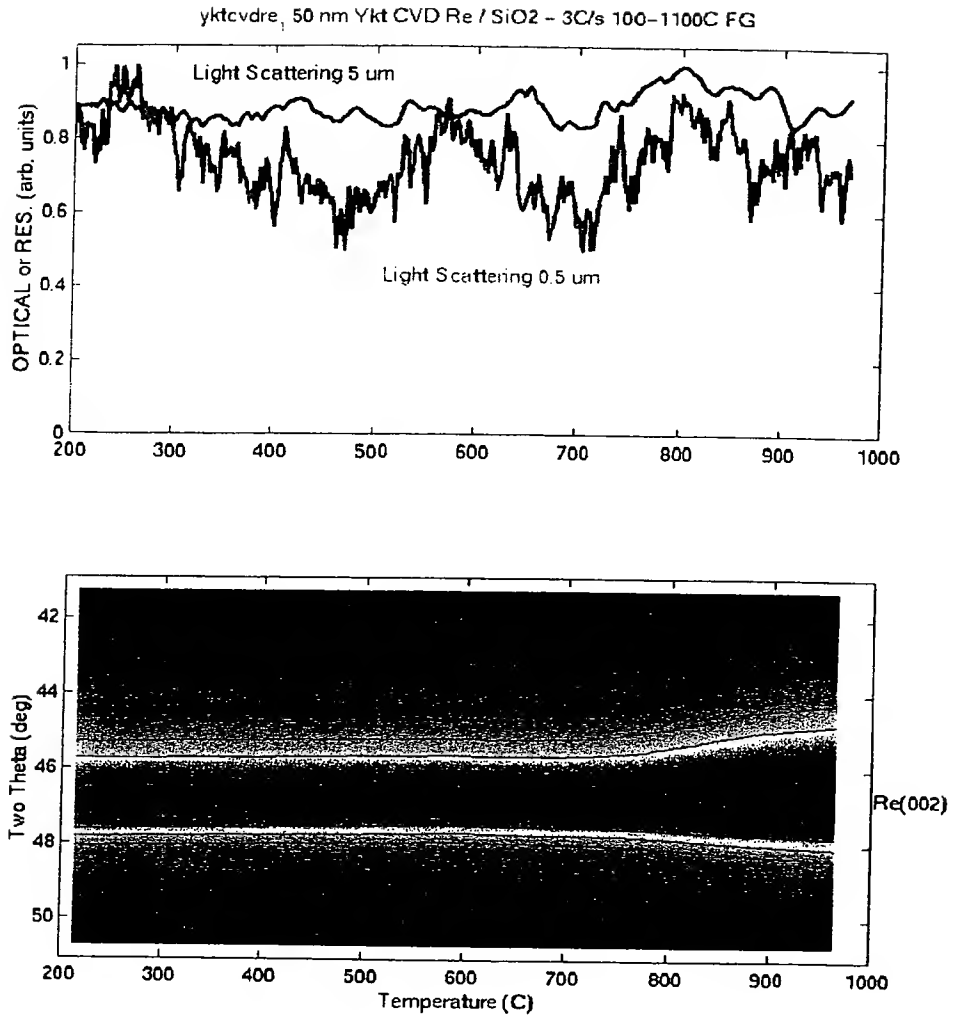

Figure 1

Figure 2 shows the results from annealing a 30 nm PVD Re film on 300 nm Al2O3 in FG at 3 C/s up to 1000 C. The contour plot (diffraction angle vs. temperature with color scale indicating x-ray intensity, dark blue lowest intensity and dark red highest intensity) follows the (002) orientation of Re as a function of temperature. Notice the peak linearly moves to lower angles on annealing due to lattice expansion. There are no indications of additional peaks or a decrease in intensity of the (002) peak which would signify a reaction with the dielectric or annealing ambient. The top plot shows the optical scattering analysis at two different lateral length scales (0.5 and 5 micro meters, red and blue curves respectively). Changes would indicate surface roughness developing in the film leading to thermal degradation. In this case no changes are seen indicating the film is not agglomerating. The black curve shows sheet resistance as a function of temperature. The initial decrease indicates some grain growth in the layer.

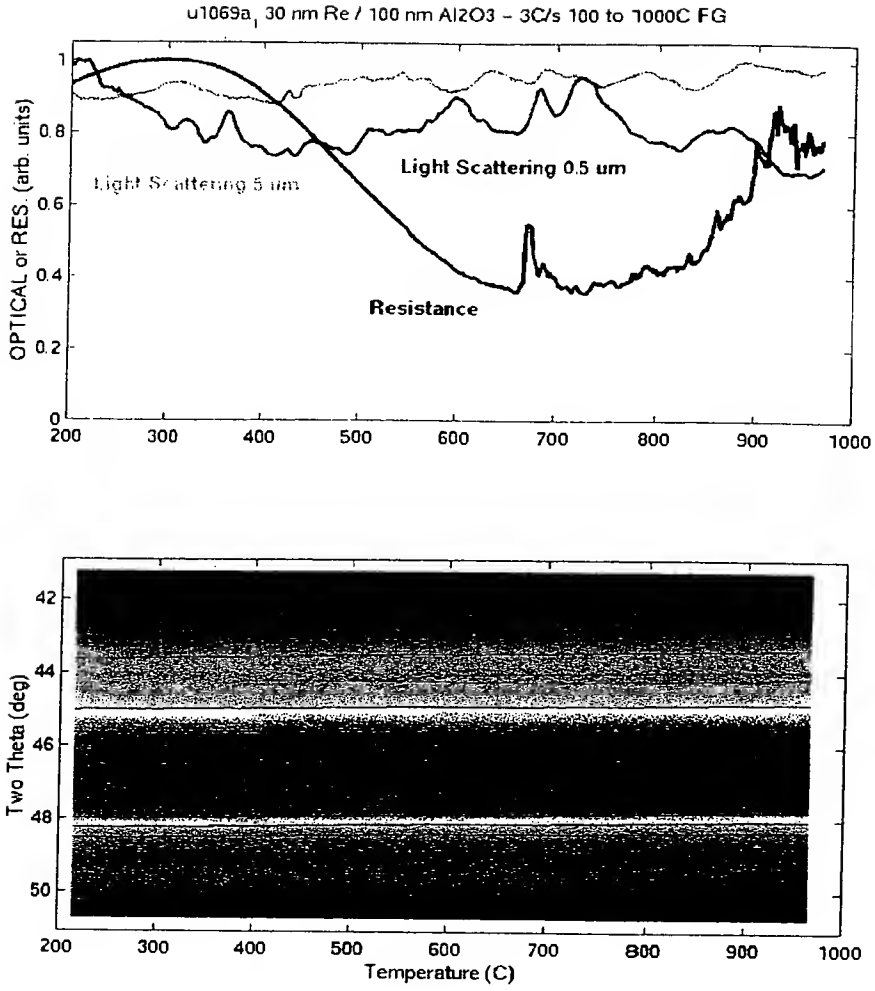

Figure 2

The time resolved techniques employed at the Brookhaven National Laboratory did not show any indication of thermal degradation or reactions for the Re, Rh, Pt and Ir gate materials in contact with SiO2 or Al2O3. The time resolved x-ray diffraction technique would only be sensitive to a reaction between the gate metal and dielectric which forms an interlayer greater than about 4-5 nm in thickness. As a finer check to determine if there was an interaction at the interface, x-ray reflectivity analysis was used. With this technique, also conducted at the Brookhaven National Laboratory, we are able to see roughness changes at the metal - dielectric interface on the order of a few angstrom's which would indicate and interaction. The technique also allows us to determine the thickness of the layers present and in that manner we can monitor if the dielectric layer gets thinner or if a third interlayer forms which would again indicate an interaction between the metal and dielectric. A further result this technique provides is an indication of the surface roughness of the films. Table 1 below summarizes the results. The first thing to note is that as-deposited the CVD Re films have a 6-7 times higher surface roughness. After a 450 C / 30 min. FG anneal treatment the interface roughness of the Re, Rh and Ir samples increases only slightly indicating very little interaction between the metal and dielectric. The Pt film actually became smoother after the FG anneal treatment. For the Re films on both SiO2 and Al2O3 there was no change in the dielectric thickness after the FG anneal treatment. These results again confirm that there is no interaction between Re, Rh, Pt and Ir gate metal materials and the dielectric after a 450 C FG anneal

treatment. As an example of interlayer formation, if titanium, a very reactive material, is used as the gate metal, after the FG anneal treatment, an interlayer is clearly seen indicating a reaction between the metal an dielectric.

X-ray Reflectivity Measurements of Metal Gate and Gate Oxide Materials

Surface Roughness Interface Roughness

Material	as dep.	after anneal (FG 450 C / 30 min.)	comments
CVD Re / SiO2	σ~30-40 A	Re slightly rougher	no change in SiO2 thickness
PVD Re / SiO2	σ~7 A	Re slightly rougher	no change in SiO2 thickness
CVD Re / Al2O3	σ~43-49 A	Re slightly rougher	no change in Al2O3 thickness
PVD Re/Al2O3	σ~8-9 A	Re slightly rougher	no change in Al2O3 thickness
PVD Rh / SiO2		Rh slightly rougher	
Ir / SiO2		Ir slightly rougher	
Pt / SiO2		Pt slightly smoother	

Table 1

Figure 3 shows that PVD 30 nm films of Re, Rh, Pt and Ir after undergoing various thermal treatments (annealing in FG at 3 C/s to 450, 550, 750 and 1000 C) maintain resistivities below 50 micro Ohm-cm. The plot on the left shows the results for films deposited on 500 nm SiO2 and that on the right on a 300 nm Al2O3 dielectric. These results indicate that the films are thermally stable and can be used in a standard high temperature integration scheme not only as the gate contact but also as local interconnects.

Resistivity of Thermally Stable Metal Gate Materials for pFET Contacts

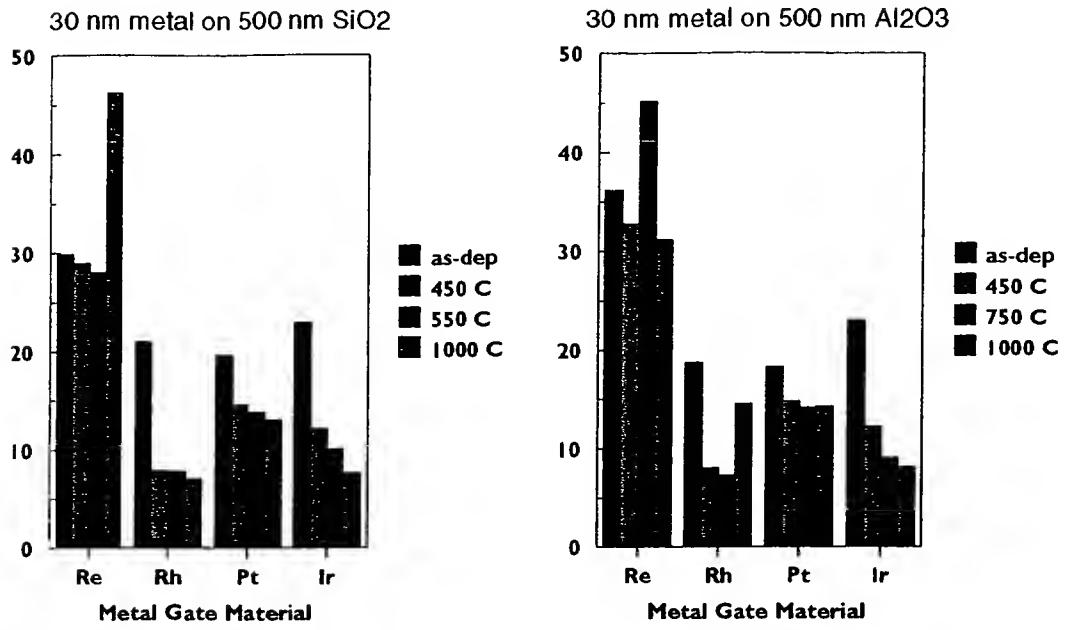

Figure 3

The CVD deposited Re films on SiO2 show strong 0002 texture as shown in Fig. 4 with an x-ray diffraction analysis. The textured films were observed independent of growth temperature for films with thicknesses less than 100 nm. The top plot in Fig. 4 shows a standard theta / two theta x-ray diffraction diffractogram which indicates the strong 0002 textured peak at about 40 deg. two theta. The lower plot shows a chi scan (fiber plot) further indicating the textured nature of the film.

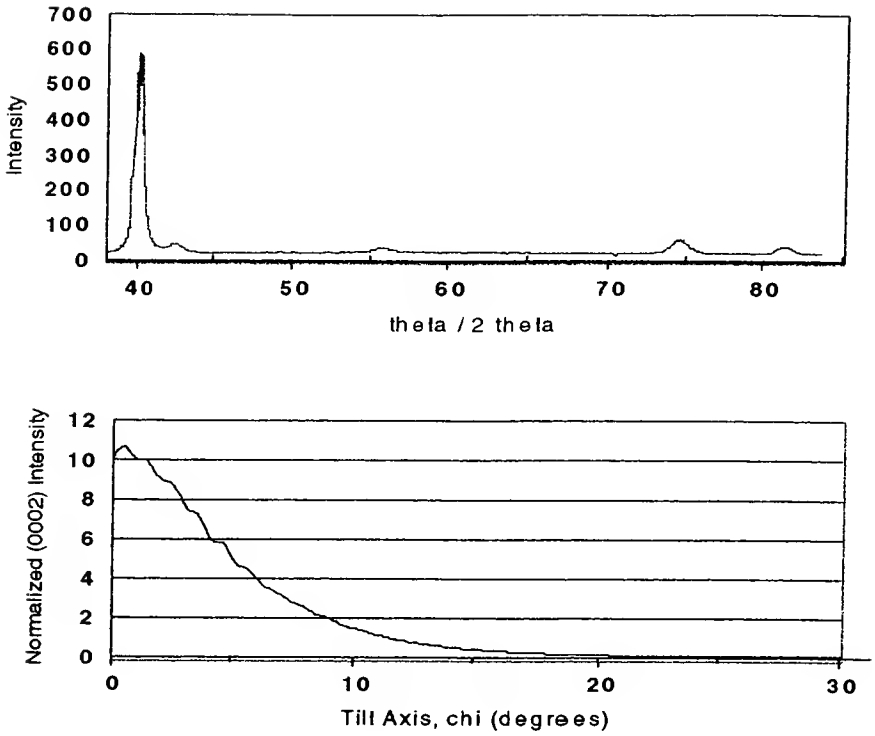

Figure 4

Deposition techniques - Acceptable deposition processes which lead to minimal gate dielectric damage and minimal long term reliability problems include thermal evaporation (from Knudsen cells) and chemical vapor deposition (CVD). Other PVD processes such as sputtering and e-beam evaporation lead to dielectric damage which is thought to be a long term reliability problem even if some damage may be repaired by a FG or H anneal treatment. CVD has the advantage over thermal evaporation in the it can be used to fill higher aspect ratio damascene features allowing for a wider variety of integration schemes. A Re CVD process has been developed using a dirhenium decacarbonyl, Re2(Co)10, precursor.

It is emphasized that the deposition of Re using CVD techniques is already known in the art. However, the deposited Re films using halide precursor causes problems of halogen incorporation and the growth temperature was usually high and the previous attempt to grow using HRe(CO)5 resulted in films with high carbon concentrations. Another attempt using Re2(CO)10 was done at high temperature about 500 °C and the properties of films were untested.

Despite the potential use of rhenium carbonyl in wiring applications, there is no disclosure of using Re2(CO)10 as the CVD source material for providing p-channel Re gates on dielectric materials such as ultra-thin gate dielectric materials.

The Re electrode fabrications in the current invention are achieved by using a low temperature/low pressure CVD technique with Re2(CO)10 as the source material. Specifically, the method of the present invention comprises the steps of: (a) depositing a uniform layer of Re directly onto a dielectric material such as an ultra-thin gate dielectric material, said dielectric material being positioned on a semiconductor substrate, said deposition is carried out by CVD using Re2(CO)10 as the source material under conditions which are sufficient to form said Re layer; and (b) patterning the structure formed in step (a) using simple patterning process including Al deposition and selective wet etching of the

structure or standard lithographic techniques to form a test capacitors or MOS device containing said p-channel Re gate on said dielectric material. It is emphasized that no chemical activation step is required in the present invention to deposit the Re layer onto the dielectric material. The present invention also provides MOS devices such as FETs which comprise at least one p-channel Re gate prepared in accordance with the method of the present invention. The devices of the present invention exhibit gate leakage comparable to prior devices prepared in accordance with existing technology and they exhibit the theoretical value for metal-gate workfunction. In accordance with this embodiment of the present invention, the Re electrode is fabricated by a method which comprises the steps of: (a) depositing a layer of Re onto a dielectric material, wherein said deposition is carried out by chemical vapor deposition (CVD) using Re2(CO)10 as a source material; (b) patterning said Re layer to form said Re electrode on said dielectric material; and (c) passivating Re and dielectric materials using conventional forming gas annealing or high pressure hydrogen to produce very low interface charge density device structure.

The present invention provides a method of fabricating p-channel Re gates directly onto dielectric materials which are present on MOS devices. The p-channel Re gates produced in accordance with the present method are compatible with ultra-thin gate dielectric materials found on MOS devices and have resistivity values close to the ideal bulk value.

In accordance with the method of the present invention, a layer of Re is directly deposited on the surface of a dielectric material which is on top of a semiconductor substrate by employing CVD using Re2(CO)10 as the source material under conditions which are sufficient to form Re layer on the dielectric material. That structure containing the Re layer is then patterned using conventional techniques well known to those skilled in the art.

The CVD apparatus includes a load-lock stainless steel reactor which comprises a graphite sample holder cartridge. The reactor further includes a boron nitride heater assembly for heating the sample during deposition and two ultra-high vacuum turbo-molecular pumps for controlling the pressure during the deposition providing base pressure of 10-7 torr.

The source material, dirhenium decacarbonyl, Re2(CO)10, is introduced into reactor chamber via a stainless steel valve and is directed to a test wafer which is contained within reactor. The source material, Re2(CO)10, which is white solid, is contained in glass tube and maintained at a constant temperature ranging from 20 to 70 °C during he deposition. The precursor is delivered by using Ar as carrier gas and the chamber pressure during growth is controlled by flow of Ar carrier gas.

CVD of Re2(CO)10 occurs at a temperature of from about 300 °C to about 550 °C. More preferably, the CVD deposition of Re occurs at a temperature of from about 350° C to about 450 °C. The pressure of the reactor during CVD is about 3 E -2 Torr. The CVD process typically is carried out for a time period of from about 10 minutes to about 5 hrs. Higher deposition rate can be achieved by using higher precursor temperature and higher carrier gas flow.

It is noted that under the above conditions a layer of Re having a thickness of from about 2 to about 200 nm, more preferably from about 20 to about 100 nm is deposited directly onto the dielectric material.

The ultra-thin dielectrics materials employed in the present invention include SiO2, nitrided SiO2, Si3N4, metal oxides and mixtures or combinations thereof. The dielectrics employed in the present invention may be grown, deposited or reacted by using techniques well known to those skilled in the art. Of the gate dielectric materials mentioned hereinabove, SiO2, lightly nitrided SiO2 (5% or less total nitride content), Al2O3, HfO2, or ZrO2 is highly preferred at present.

After depositing the Re layer, the samples are patterned using Al as hard masks or standard lithographic techniques well known to those skilled in this art. This includes positioning photoresists on the surface of the CVD Re layer; developing the photoresists and removing, via etching techniques, those areas that do not contain the photoresists. Etching may be carried out using wet or dry techniques well known to those skilled in the art. When wet etching is employed, the chemical etchant is selected from the group consisting of H2O2, chromic acid, phosphoric acid, acetic acid, and the like thereof. The preferred chemical etchant employed in the present invention is H2O2. When dry chemical etching is employed in the present invention, it may be carried out by reactive ion etching (RIE), ion beam etching (IBE) or laser ablation. Each of the aforementioned dry etching techniques are well known to those skilled in the art.

Test structures were fabricated using thermally grown silicon dioxide thin films ranging in

thicknesses from 2.0-20.0 nm to form MOS capacitors. Additional experiments were performed on device structure wafers containing dielectric thickness from 1 to 2 nm and on Al2O3 layers grown by molecular beam epitaxy. Films were grown on p-type or n-type wafers with resistivities of about 0.1 to 0.2 ohm-cm. Re films were deposited on the test wafers in blanket fashion. Specifically, Re deposition was carried out in a load-locked, stainless steel reactor with a base pressure of about 10-7 torr. Dirhenium decacarbonyl, Re2(CO)10, was used as the source gas and it was emitted into the reactor via a stainless steel valve and directed onto the sample. The precursor delivery rate was controlled by using Ar as carrier gas. The samples were introduced on a graphite sample holder cartridge which in turn was introduced into a heater assembly located within the reactor chamber. The deposition was conducted at a temperature range of 300-550 °C. The growth rate in the system was typically about 0.1 to 1.5 nm/minute depending on precursor and deposition temperature.

Electrical characterization - For a gate metal pFET contact a work function within ~0.2 eV from the valance band edge (Ev) is necessary. The work function for the Re metal gate material was established to be 4.6 to 5.0 eV. Besides the work function another important consideration is the interface trapped charge which can be minimized after deposition by a hydrogen anneal treatment. The conventional treatment is a FG anneal but a new process using 400 Torr of Hydrogen and 350 C has shown superior results. For the Re gate metal the interface trapped charge (Dit) was reduced to 3-4 E 10 /cm-2 * eV-1 with the use of high hydrogen pressures necessary to produce properly passivated interfaces without the material undergoing chemical changes.

After deposition of the Re films, capacitors were patterned using evaporated 60 nm thick Al dots as hard mask for wet etching. The rhenium film on each device was wet-etched using H2O2. Capacitor structures were thus formed with areas ranging from about 1 E -6 to about 1 E -2 cm . Additionally, Re films were patterned by wet etching using standard lithography techniques for device structure wafers.

The capacitors prepared above were tested using high frequency and quasi-static capacitance-voltage (C-V) and current-voltage (I-V) techniques. FIG. 5 show typical C-V data for Re gate capacitors structures formed having a thickness of about 4.3 nm capacitor. Data is shown for capacitor formed on n-type silicon wafers. The dotted and solid lines show the C-V data before and after a standard post metal gate deposition forming gas anneal (FGA) step which is carried out in 10% H in nitrogen at 400 °C for about 30 minutes.

Analysis of the C-V data show interface state densities in the low 3-4 E 11 cm-2eV-1 for samples subjected to FGA. The flat band voltage is approximately 0.5 eV. This, in itself, demonstrate that the Fermi-level of the metal gate is situated very close to silicon valence band edge indicating that Re gate is appropriate choice for p-FET MOS structure. The as-dep sample has some defects state as seen in FIG. 5 but can be easily removed by standard FGA step. C-V data were obtained for other Re gate capacitors with dielectric thickness ranging from 2-20 nm and the work function was evaluated as 5.0 eV.

Although the conventional FGA produces acceptable range of interface state density, it can be even improved by using newly developed high pressure H2 annealing process. The process is performed in the load lock chamber using a He lamp heater. The patterned samples are located in the chamber and maintained at 350 °C and high pressure H2 is introduced, typically 400 Torr for 30 minutes. By this process, the interface state densities are reduced to low (3-4) E 10 cm-2*eV-1. FIG 6 shows typical high frequency and quasi-static C-V data for Re gate capacitors structures having an oxide thickness of about 20 nm capacitor after the high pressure annealing process.

C-V and I-V data for device structure wafers employing Re gates having oxide thickness of 2 nm are shown in FIGS. 7 and 8. The dotted and solid lines show the C-V and I-V data before and after a standard FGA step. These data demonstrates that the Re gate capacitors work on thin 2 nm gate dielectrics and have leakage currents as low as those of standard polysilicon based capacitors.

FIG 9 shows C-V data for Re gate capacitors structures formed on Al2O3 dielectrics having a thickness of about 6 nm. The capacitor is formed on an n-type silicon wafer. The flat band voltage was about 0.48 eV, which is essentially the same as on SiO2. This indicates the Re can be used as electrode material for p-channel metal gates using Al2O3 as dielectric.

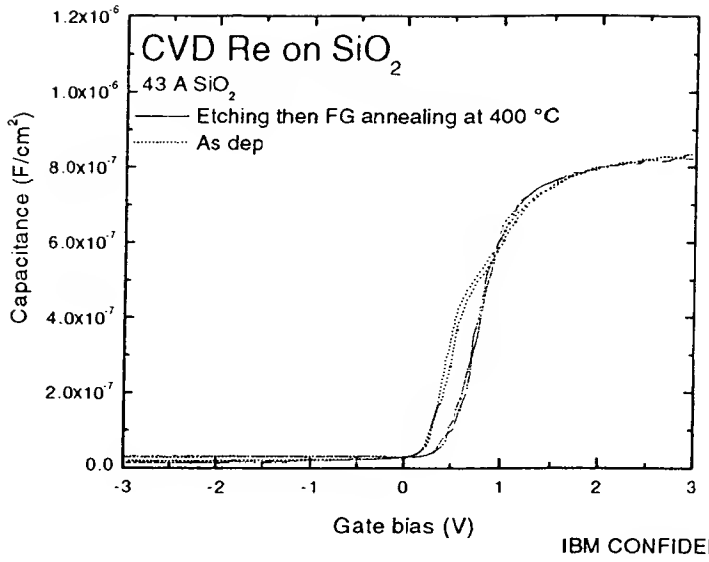

FIG. 5 is a capacitance-voltage diagram for a Re gate capacitor structure formed in accordance with the present invention having a thickness of 4.3 nm. Dotted line as grown; solid line after FGA.

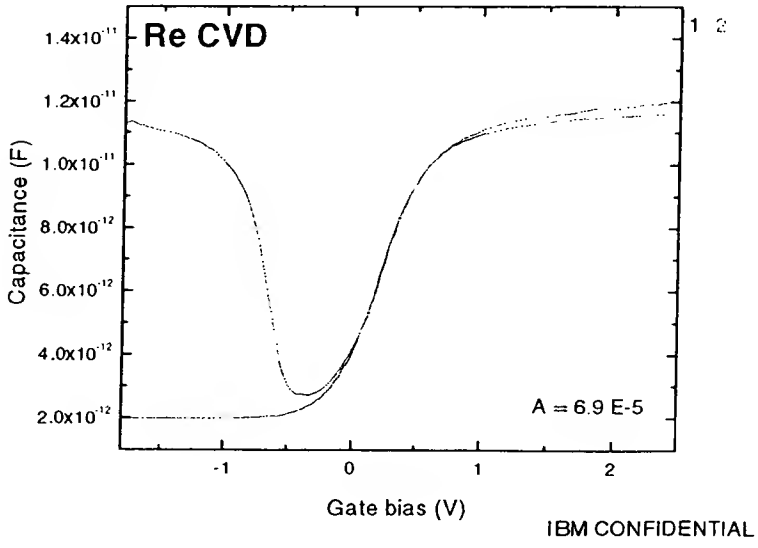

FIG. 6 is a high frequency and quasi-static capacitance-voltage diagram for a Re gate capacitor structure formed in accordance with the present invention having a thickness of 20 nm after high pressure H2 annealing.

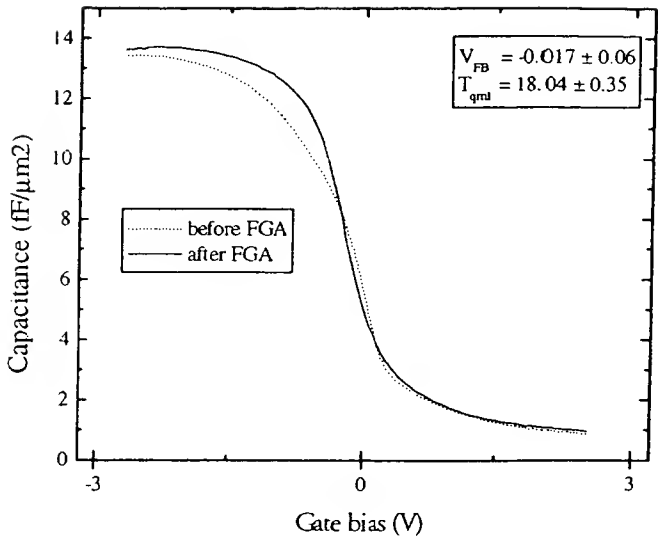

FIG. 7 is a high frequency capacitance-voltage diagram for a Re gate device structure formed in accordance with the present invention having a thickness of 2.0 nm. Dotted line as grown; solid line after FGA.

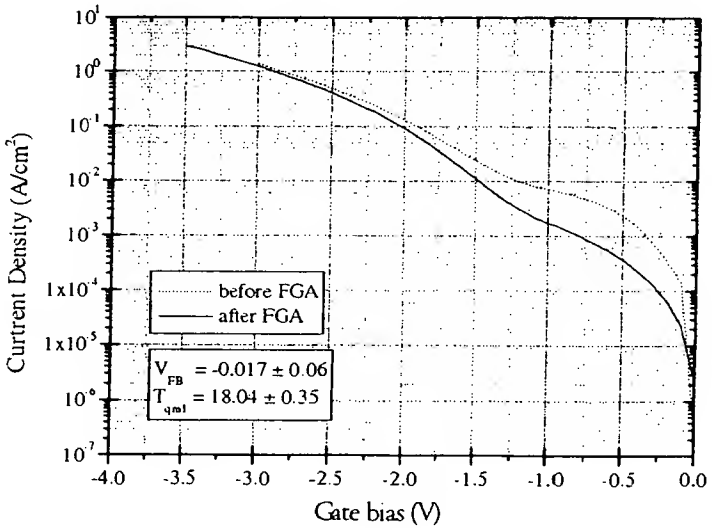

FIG 8 is a current-voltage diagram for a Re gate device structure formed in accordance with the present invention having a thickness of 2.0 nm. Dotted line as grown; solid line after FGA.

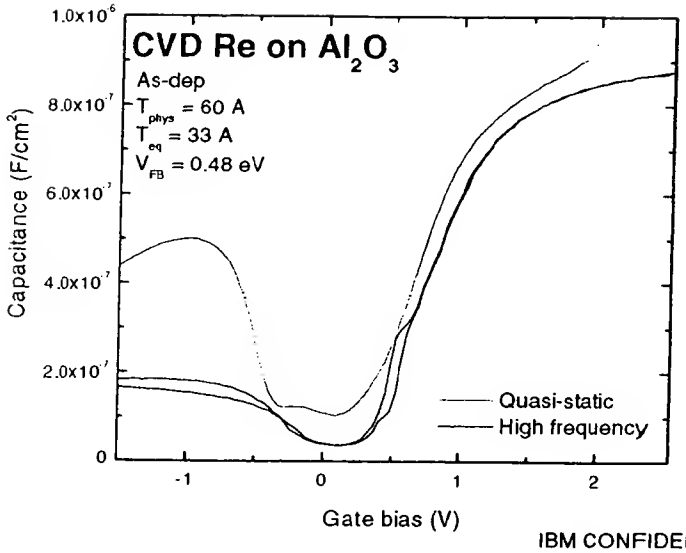

FIG. 9 is a high frequency and quasi-static capacitance-voltage diagram for a Re gate capacitor structure formed in accordance with the present invention on Al2O3 film having a thickness of 6 nm after FGA.

Integration - The integration scheme chosen will determine the maximum temperature the gate metal / dielectric will have to withstand. For a standard CMOS process for which the dielectric and poly-Si contact are in place before the source and drain activation anneals the stack will have to withstand 1000 C thermal treatments. As mentioned above Re, Rh, Pt, Ir and Ru and can withstand such treatments without thermal degradation. Two additional possible integration schemes include having the metal / dielectric combination in place before source and drain silicide formation but not before the activation anneals. In this case the combination would have to withstand anneal treatments at 750 C for CoSi2 formation. In the last integration scheme the standard process is followed (i.e. poly-Si flow). After the stack is built the poly-Si is etched away and the dielectric deposited followed by the metal fill (CVD process) into the damascene feature. Chemical mechanical polishing (CMP) is then used to planarize the structure. In this scheme the maximum processing temperature is 400 C.

Sample Claims

Device:

1) A MOS device comprising at least one pFET work-function material (Re, Rh, Ir, Pt, Ru) gate on an ultra thin dielectric material, said ultra-thin dielectric material having the primary gate leakage current due to direct tunneling, wherein said pFET work-function material is formed by
(a) depositing a layer of the pFET work-function material onto said ultra-thin gate dielectric material, said ultra-thin gate dielectric material being positioned on a semiconductor substrate and said deposition process being carried out by chemical vapor deposition (CVD) using (Re2(CO)10) as a source material;
(b) patterning the structure formed in step (a).

2) A field effect transistor (FET) comprising at least one pFET work-function material (Re, Rh, Ir, Pt, Ru) gate on an ultra thin dielectric material, said ultra-thin dielectric material having the primary gate leakage current due to direct tunneling, wherein said pFET work-function material is formed by
(a) depositing a layer of the pFET work-function material onto said ultra-thin gate dielectric material, said ultra-thin gate dielectric material being positioned on a semiconductor substrate and said deposition process being carried out by chemical vapor deposition (CVD) using (Re2(CO)10) as a source material;

(b) patterning the structure formed in step (a).

3) The MOS device of claim one wherein said ultra-thin gate dielectric material is selected from the group consisting of SiO2, nitrided SiO2, Si3N4, metal oxides and mixtures thereof.

4) The MOS device of claim one wherein said ultra-thin gate dielectric material is selected from the group consisting of Al2O3, HfO2, ZrO3, Si3N4 and mixtures thereof.

5) The MOS device of claim three wherein said ultra-thin dielectric is SiO2.

6) The MOS device of claim one wherein said semiconductor substrate contains at least one source and drain region.

7) The MOS device of claim six wherein said semiconductor substrate is p-type or n-type.

8) The MOS device of claim seven wherein said semiconductor substrate is composed of silicon, SiGe, SOI or GaAs.

9) The MOS device in claim eight wherein said semiconductor substrate is silicon.

10) The FET device of claim two wherein said ultra-thin gate dielectric material is selected from the group consisting of SiO2, nitrided SiO2, Si3N4, metal oxides and mixtures thereof.

11) The FET device of claim two wherein said ultra-thin gate dielectric material is selected from the group consisting of Al2O3, HfO2, ZrO3, Si3N4 and mixtures thereof.

12) The FET device of claim ten wherein said ultra-thin dielectric is SiO2.

13) The MOS device of claim two wherein said semiconductor substrate contains at least one source and drain region.

14) The MOS device of claim thirteen wherein said semiconductor substrate is p-type or n-type.

15) The MOS device of claim fourteen wherein said semiconductor substrate is composed of silicon, SiGe, SOI or GaAs.

16) The MOS device in claim fifteen wherein said semiconductor substrate is silicon.

Method:

1) Method for forming at least one pFET Re, Rh, Pt, Ir or Ru metal contact in a semiconductor device comprising the following:
a) positioning a preprocessed semiconductor substrate in a chemical vapor deposition chamber;
b) depositing a uniform layer of Re directly onto a dielectric material such as an ultra-thin gate dielectric, said ultra-thin dielectric material having the primary gate leakage current due to direct tunneling, said dielectric material being positioned on a semiconducting substrate, said deposition is carried out by CVD using Re2(Co)10 as the source material under conditions which are sufficient to form said Re layer;
c) patterning said Re layer to form said Re electrode on said dielectric material;
d) passivating said Re and dielectric materials using conventional forming gas annealing or high pressure hydrogen process to produce low interface change density device structure.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures in-line as appropriate)?

The new pFET material solves two issues. The first is polycrystalline silicon depletion which reduces the effective capacitance of poly-Si gate devices, and necessitates the use of a thinner dielectric than would otherwise be required. The depletion in the poly-Si can be thought of as adding several angstrom's of oxide thickness to the dielectric. The second issue is the compatibility with high-k dielectrics (Al2O3, HfO2, ZrO2). Poly-Si tends to react with the high-k materials during processing which renders it unusable. The metal gate materials overcome this problem being stable on the high-k dielectric materials. The thermal stability (no interaction with the dielectric) makes it fully compatible with standard post processing techniques, e,g. activation anneals and the like.

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?
The problem is generally known, but there are no fully satisfactory solutions extant.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.
N/A